APM32F407

Errata Sheet

Version: V 2.0

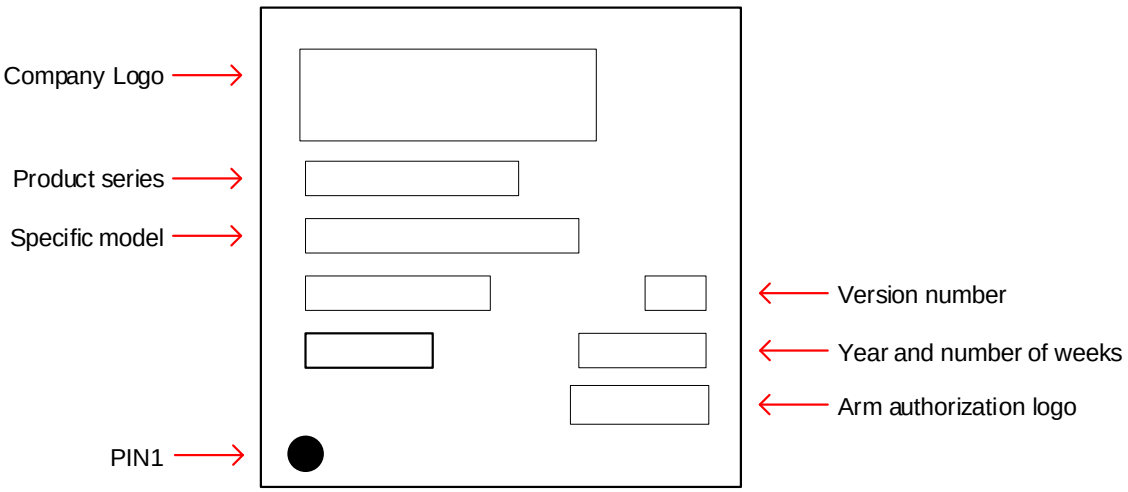
Contents

1 Introduction

This Manual mainly introduces the limitations of the APM32F407 series products during use. If you encounter the application scenarios described in the manual during the use of the product, please use the product according to the solutions provided in the manual; if no solution is provided, please avoid this application scenario.

2 Product Version and Silk Screen Printing Instructions

Figure 1 Product Version and Silk Screen Printing Instructions



3 Errata List

Table 1 Errata List

Category	Introduction	Product version			
		A2	A3	C1	C2
Power Management	PDR_ON pin functions	●	●	●	●
	Power Consumption	●	●	×	×
	BOR level setting	●	●	×	×
Flash	Erase Flash and interrupt	●	×	×	×
	FLASH erase by mistake	●	×	×	×
	Abnormal running of Flash configuration in SRAM	●	●	●	●
Bootloader	Bootloader ISP upgrade	●	●	×	×
Interrupt	Priority grouping	●	●	×	×
	Priority shielding	●	●	×	×
	System processing priority	●	●	×	×
GPIO	PB pin level delay	●	●	●	●
SPI	I2S full duplex mode	●	●	●	●
USB	LS host mode of USB_OTG_FS module	●	●	●	●
	USB_OTG_HS2 device mode low-power wake-up	●	●	●	●
Simulator	J-Link simulating download program	●	●	●	●

Note: "●" indicates that this errata description is involved in this version; the 'X' indicates that it is not involved in this version.

4 Power Management

4.1 PDR_ON pin functions

Problem description

The PDR_ON pin controls the function of the internal power supply detection resetting. Enable the pin high level, and all POR/PDR/PVD/VBAT functions can be used normally. Enable the pin low level, the above functions will be disabled, but the POR/PDR/PVD/VBAT functions can still be used normally.

Solutions

Disable the BOR detection function, and when the PDR_ON pin level is pulled low, the POR/PDR function is disabled, but the PVD/VBAT function is not affected.

4.2 Power Consumption

Problem description

When entering the stop or standby mode, the EMMC clock will not be automatically turned off. If the EMMC clock is enabled before entering the stop or standby mode, after entering the stop or standby mode, the EMMC clock will still be in the enabled state, and the power consumption of the stop or standby mode will include the power consumption of EMMC.

Solutions

Before entering the stop or standby mode, if the EMMC clock is enabled, the AHB3 peripheral clock needs to be configured to enable the register (RCM_AHB3CLKEN) and disable the EMMC clock , and then it can enter the stop or standby mode.

4.3 BOR level setting

Problem description

The undervoltage reset level in the option byte can be configured to modify the undervoltage reset threshold. After the option byte is configured, the BOR level needs to be reset to take effect.

Solutions

Choose either of the following solutions:

- Take effect through reset;
- Solve related problems by migrating the C1 version.

5 Flash

5.1 Erase Flash and interrupt

Problem description

When the prefetch buffer, I-cache, and D-cache are enabled, if the flash erase/write process is interrupted, the program may run abnormally.

Solutions

Turn off the interrupt before erasing/writing Flash, and turn on the interrupt after erasing/writing Flash is completed.

5.2 FLASH erase by mistake

Problem description

There are two situations for Flash erase by mistake:

- In the case of IAP, conduct page erase by writing option bytes and the UID of the chip will be erased.
- When erasing/writing the main memory block Flash after erasing/writing the option bytes, the information of chip configuration such as UID and HSI Trimming will be erased. As a result, all read UID will be 0xFFFFFFFF, and the accuracy deviation of HSI will be significant, rather than ±1% accuracy calibrated before leaving the factory.

Solutions

Choose either of the following solutions:

- If a user program is executed, after erasing/writing the option byte and before erasing/writing the main memory block Flash, insert the following operation:
  (1) Unlock the main memory block Flash;
  (2) Write data 0x08 to the address 0x40023C30;
  (3) Read FMC_STS_BUSY and wait for it to be cleared to 0;
  (4) Lock the main memory block Flash.

  After completing the above operations, erase/write the main memory block Flash.
- If a programmer is used to erase/write the option bytes and erase/write the main memory block Flash, after completing erasing/writing the option bytes, the programmer needs to reset the MCU, and then the main memory block Flash can be erased/written.
- Related problems can be solved by migrating the C1 version.

5.3 Abnormal running of Flash configuration in SRAM

Problem description

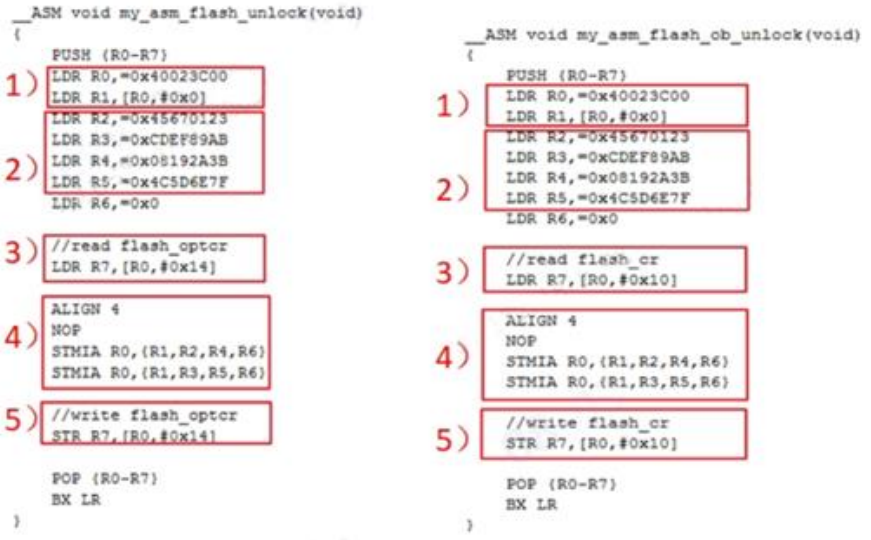
This problem only arises in specific scenarios where CPU performs the fetch instructions from the offset address of SRAM 0x040 while performing the Flash unlock operation. This scenario often involves the Flash registers with an offset address of 0x040.

Solutions

Modify the software driver and implement FLASH_UNLOCK/OPTUNLOCK using assembly. The specific operating method is as follows:

Use the multi-word storage instruction stmia to write the FLASH_KEYR/OPTKEYR registers, writing four registers at once, to ensure that the CPU does not issue prefetch instruction during write operation of 0x40023C04 (FLASH_KEYR address), and 0x40023C08 (FLASH_OPTKEYR address).

Figure 2 Assembly-based Flash Unlock Operation



Unlocking process:

1) Read the value of FLASH_ACR and wait for the data to be written once to prevent rewriting of FLASH_ACR.

2) Write the values of FLASH_KEY1, FLASH_KEY2, FLASH_OPTKEY1 and FLASH_OPTKEY2 to r2~r5.

3) Read FLASH_OPTTCR/CR to prevent rewriting of the FLASH OPTUNLOCK/UNLOCK status.

4) Insert the pseudo instruction ".align 4\n" to align the address of the next instruction with 4, and then insert the nop instruction to align the addresses of two stmia instructions with 2.

5) Write FLASH_OPTTCR/CR to restore the FLASH OPTUNLOCK/UNLOCK state.

6 Bootloader

6.1 Bootloader ISP upgrade

Problem description

When the chip is in bootloader mode, it cannot perform normal ISP upgrades using 25M HSE during CAN communication.

Solutions

Choose either of the following solutions:

- In bootloader mode, the HSE with a frequency of 25MHz is not used to conduct CAN communication for ISP upgrade, but the HSE of other frequency can be used, for example, using 16HMz HSE to conduct CAN communication for ISP upgrade.
- Related problems can be solved by migrating the C1 version.

7 Interrupt

7.1 Priority grouping

Problem description

The significant bits of the interrupt priority register (NVIC_IPRx) are Bits [7:5], supporting 8 programmable priorities and the available programmable

priority levels are: 0x00, 0x20, 0x40, 0x60, 0x80, 0xA0, 0xC0, and 0xE0.

Support 4 types of priority groups, and the definition of PRIGGROP[2:0] is as follows:

PRIGROUP [2:0]	Interrupt priority level value, PRI_N[7:5]			Number of	
	Binary point	Group priority bits	Subpriority bits	Group priorities	Sub priorities
0b011	None				
0b100	0bxxx	[7:5]	None	8	None
0b101	0bxx.y	[7:6]	[5]	4	2
0b110	0bx.yy	[7]	[6:5]	2	4
0b111	0b.yyy	None	[7:5]	Non	8

Solutions

Related problems can be solved by migrating the C1 version.

7.2 Priority shielding

Problem description

The significant bits of the basic priority mask register BASEPRI are Bits [7:5], which support 3-bit programmable basic priority masking. The configurable masking priority levels are: 0x20, 0x40, 0x60, 0x80, 0xA0, 0xC0, and 0xE0.

Solutions

Related problems can be solved by migrating the C1 version.

7.3 System processing priority

Problem description

The significant bits of the system processing priority register (SCB_SHPRx) are Bits [7:5], which support 3-bit programmable system processing priority.

Solutions

Related problems can be solved by migrating the C1 version.

8 GPIO

8.1 PB pin level delay

Problem description

When PB14 and PB15 pins switch from push-pull output high level to pull-down input mode at room temperature, they cannot be pulled down to 0V. After the temperature rises to a high temperature of 120°C, it can be pulled down to 0V, but the waveform of the pin pull-down input is abnormal.

The specific operation scenario is to configure the I/O of PB14 and PB15 as push-pull pull-up output high level, and switch the pull-down input mode:

- At room temperature, a delay of 100ms is required to pull down to 0V, but the waveform is abnormal, and a delay of 3s is needed to stabilize the low-level 0V.
- At a high temperature of 120°C, a delay of 500us is required to pull down to 0V, but the waveform is abnormal.

Solutions

It is suggested that the PB14 and PB15 pins should not use the operation sequence of switching to pull-down input after push-pull output high level.

After the push-pull output high-level is completed, insert the push-pull low-level output or configure as open-drain output mode, and then switch to pull-up input mode.

9 SPI

9.1 I2S interface

9.1.1 I2S full-duplex mode

Problem description

In I2S2 full-duplex mode, after I2S2_SCK remaps P11, and I2S2_WS remaps PI0, I2S2 cannot transmit or receive data.

Solutions

Remap the SCK and WS signals to the following other PB pins:

- I2S2 CK signal: PB10 or PB13 pin
- I2S2 WS signal: PB12 or PB9 pin

10 USB

10.1 USB_OTG_FS

10.1.1 LS Host Mode of USB_OTG_FS Module

Problem description

When the USB_OTG_FS module is configured as LS host mode, the eye diagram of the 5m line test is not perfect, the eye diagram of the 1m line test at 3.0V is not perfect, and the test results of both 1m and 5m lines at 2.7V are abnormal.

Solutions

It can be corrected and improved by adjusting the off-chip series resistance, for example, in case of overshoot, increase the resistance, and if the rise and fall time is slow, reduce the resistance. The test shows that, in FS mode, the off-chip resistance is 22 Ω; in LS mode, an off-chip resistance of 16 Ω is suitable.

10.2 USB_OTG_HS

10.2.1 USB_OTG_HS2 device mode low-power wake-up

Problem description

When the USB_OTG_HS2 module is configured as device mode, an exception of failure to respond to USB will occur when entering the low-power mode of MCU core, which means that it cannot wake up by the corresponding wake-up interrupt after entering the low-power mode like FS or HS1.

Solutions

It is possible to suspend DP to an external interrupt and enable the external interrupt of corresponding pin when the suspend event enters the MCU core low-power mode. When the computer wakes up, it will pull up the DP to enter the external interrupt service function, then release the core sleep in the external interrupt function, reconfigure the clock, turn on the PHY clock, turn off the external interrupt enable, and clear the external interrupt flag. For the codes, please refer to the SDK routine OTGD_HID_HS2_LowPower.

11 Simulator

11.1 J-Link simulating download program

Problem description

When using the J-Link simulator to download programs, if the J-Link driver is at version 7.00 or below and the MCU is reset in the program downloading process, the option bytes may be erased by mistake.

Solutions

Choose either of the following solutions:

- Use the driver of J-Link V7.00 or higher version;
- Avoid resetting the MCU in the process of using J-Link to download programs.

12 Revision history

Table2 Document Revision History

Date	Version	Revision History
August 2024	1.0	New edition

Statement

This document is formulated and published by Geehy Semiconductor Co., Ltd. (hereinafter referred to as “Geehy”). The contents in this document are protected by laws and regulations of trademark, copyright and software copyright. Geehy reserves the right to make corrections and modifications to this document at any time. Read this document carefully before using Geehy products. Once you use the Geehy product, it means that you (hereinafter referred to as the “users”) have known and accepted all the contents of this document. Users shall use the Geehy product in accordance with relevant laws and regulations and the requirements of this document.

1. Ownership

This document can only be used in connection with the corresponding chip products or software products provided by Geehy. Without the prior permission of Geehy, no unit or individual may copy, transcribe, modify, edit or disseminate all or part of the contents of this document for any reason or in any form.

The “极海” or “Geehy” words or graphics with “®” or “™” in this document are trademarks of Geehy. Other product or service names displayed on Geehy products are the property of their respective owners.

2. No Intellectual Property License

Geehy owns all rights, ownership and intellectual property rights involved in this document.

Geehy shall not be deemed to grant the license or right of any intellectual property to users explicitly or implicitly due to the sale or distribution of Geehy products or this document.

If any third party’s products, services or intellectual property are involved in this document, it shall not be deemed that Geehy authorizes users to use the aforesaid third party’s products, services or intellectual property. Any information regarding the application of the product, Geehy hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party, unless otherwise agreed in sales order or sales contract.

3. Version Update

Users can obtain the latest document of the corresponding models when ordering Geehy products.

If the contents in this document are inconsistent with Geehy products, the agreement in the sales order or the sales contract shall prevail.

4. Information Reliability

The relevant data in this document are obtained from batch test by Geehy Laboratory or cooperative third-party testing organization. However, clerical errors in correction or errors caused by differences in testing environment may occur inevitably. Therefore, users should understand that Geehy does not bear any responsibility for such errors that may occur in this document. The relevant data in this document are only used to guide users as performance parameter reference and do not constitute Geehy's guarantee for any product performance.

Users shall select appropriate Geehy products according to their own needs, and effectively verify and test the applicability of Geehy products to confirm that Geehy products meet their own needs, corresponding standards, safety or other reliability requirements. If losses are caused to users due to user's failure to fully verify and test Geehy products, Geehy will not bear any responsibility.

5. Legality

USERS SHALL ABIDE BY ALL APPLICABLE LOCAL LAWS AND REGULATIONS WHEN USING THIS DOCUMENT AND THE MATCHING GEEHY PRODUCTS. USERS SHALL UNDERSTAND THAT THE PRODUCTS MAY BE RESTRICTED BY THE EXPORT, RE-EXPORT OR OTHER LAWS OF THE COUNTRIES OF THE PRODUCTS SUPPLIERS, GEEHY, GEEHY DISTRIBUTORS AND USERS. USERS (ON BEHALF OR ITSELF, SUBSIDIARIES AND AFFILIATED ENTERPRISES) SHALL AGREE AND PROMISE TO ABIDE BY ALL APPLICABLE LAWS AND REGULATIONS ON THE EXPORT AND RE-EXPORT OF GEEHY PRODUCTS AND/OR TECHNOLOGIES AND DIRECT PRODUCTS.

6. Disclaimer of Warranty

THIS DOCUMENT IS PROVIDED BY GEEHY "AS IS" AND THERE IS NO WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, TO THE EXTENT PERMITTED BY APPLICABLE LAW.

GEEHY'S PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED FOR USE AS CRITICAL COMPONENTS IN MILITARY, LIFE-SUPPORT, POLLUTION CONTROL, OR HAZARDOUS SUBSTANCES MANAGEMENT SYSTEMS, NOR WHERE FAILURE COULD RESULT IN INJURY, DEATH, PROPERTY OR ENVIRONMENTAL DAMAGE.

IF THE PRODUCT IS NOT LABELED AS "AUTOMOTIVE GRADE," IT SHOULD NOT BE CONSIDERED SUITABLE FOR AUTOMOTIVE APPLICATIONS. GEEHY ASSUMES NO LIABILITY FOR THE USE BEYOND ITS SPECIFICATIONS OR GUIDELINES.

THE USER SHOULD ENSURE THAT THE APPLICATION OF THE PRODUCTS COMPLIES

WITH ALL RELEVANT STANDARDS, INCLUDING BUT NOT LIMITED TO SAFETY, INFORMATION SECURITY, AND ENVIRONMENTAL REQUIREMENTS. THE USER ASSUMES FULL RESPONSIBILITY FOR THE SELECTION AND USE OF GEEHY PRODUCTS. GEEHY WILL BEAR NO RESPONSIBILITY FOR ANY DISPUTES ARISING FROM THE SUBSEQUENT DESIGN OR USE BY USERS.

7. Limitation of Liability

IN NO EVENT, UNLESS REQUIRED BY APPLICABLE LAW OR AGREED TO IN WRITING WILL GEEHY OR ANY OTHER PARTY WHO PROVIDES THE DOCUMENT AND PRODUCTS "AS IS", BE LIABLE FOR DAMAGES, INCLUDING ANY GENERAL, SPECIAL, DIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE DOCUMENT AND PRODUCTS (INCLUDING BUT NOT LIMITED TO LOSSES OF DATA OR DATA BEING RENDERED INACCURATE OR LOSSES SUSTAINED BY USERS OR THIRD PARTIES). THIS COVERS POTENTIAL DAMAGES TO PERSONAL SAFETY, PROPERTY, OR THE ENVIRONMENT, FOR WHICH GEEHY WILL NOT BE RESPONSIBLE.

8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.